CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory cell, comprising:

a substrate, said substrate including a source region and a drain region;

a first insulating layer over said substrate;

a first conductive layer over said first insulating layer;

a programmable conductance element over said first electrode, said programmable conductance element having a resistance which is controllable between at least two states; and

a second conductive layer over said programmable conductance element.

2. The memory cell of claim 1, wherein said programmable conductance element is comprised of a chalcogenide glass.

3. The memory cell of claim 2, wherein said chacogenide glass is comprised of germanium-selenide.

4. The memory cell of claim 2, wherein said chacogenide glass comprises Ge_xSe_{100-x}.

5. The memory cell of claim 4, wherein x has a range of from 18 to 43.

6. The memory cell of claim 5, wherein x is 20.

7. The memory cell of claim 2, wherein said chacogenide glass is doped with a metal.

8. The memory cell of claim 2, wherein said chacogenide glass is doped with silver.

9. The memory cell of claim 1, wherein said first and second conductive layers are comprised of one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

10. A method for forming a memory cell, comprising:

forming a source region in a substrate;

forming a drain region in the substrate;

forming a first insulating layer over the substrate;

forming a first conductive layer over the first insulating layer;

forming a programmable conductance element over the first electrode; and

forming a second conductive layer over the programmable conductance element,

wherein said programmable conductance element has a resistance which is controllable between at least two states.

11. The method of claim 10, wherein said programmable conductance is comprised of a chalcogenide glass.

12. The method of claim 11, wherein said chacogenide glass is comprised of germanium-selenide.

13. The method of claim 11, wherein said germanium-selenide comprises Ge_xSe_{100-x}.

14. The method of claim 13, wherein x has a range of 18 to 43.

15. The method of claim 14, wherein x is 20.

16. The method of claim 11, further comprising:

doping said chacogenide glass with a metal.

17. The method of claim 16, wherein said metal is silver.

18. The method of claim 10, wherein said first and second conductive layers are formed from a group of metals comprising one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

19. A method for writing or erasing data into a memory cell having a gate stack including a programmable conductor disposed between a first conductive layer and a second conductive layer, the gate stack being disposed between a source and a drain region of the cell, said method comprising:

changing a resistance of the programmable conductance element between said first and second electrodes to a first state by forming a conductance between the first and second electrodes.

20. The method of claim 19, wherein changing the resistance comprises:

applying a first voltage to the second electrode; and

applying a second voltage to the source.

21. The method of claim 20, wherein said first voltage is about 8 volts to about 12 volts.

22. The method of claim 21, wherein said second voltage is about 6 volts.

23. A method for reading a memory cell having gate stack including a programmable conductance element disposed between a first conductive layer and a second conductive layer, the gate stack being disposed between a source and a drain region of the cell, said method comprising:

applying a reading voltage to said second electrode, wherein said reading voltage is selected to cause an inversion layer to form between said source and said drain only if said memory cell is in a first predetermined state; and

sensing the presence or absence of the inversion layer.

24. The method of claim 23, further comprising:

precharging a target bit line to a first predetermined potential level;

precharging a reference bit line to a second predetermined potential level;

coupling said target bit line to said memory cell while said reading voltage is active; and

sensing a voltage difference between said target bit line and said reference bit line.

25. The method of claim 24, further comprising:

applying a small forward bias to said target bit line.

26. A memory device, comprising:

a control circuit;

a memory array, coupled to said control circuit, said memory array further comprising a plurality of blocks, each of said plurality of blocks including a plurality of memory cells,

wherein each of said memory cells comprises,

a substrate, the substrate having a source region and a drain region;

a first insulating layer over said substrate;

a first conductive layer over said first insulating layer;

a programmable conductance element over said first electrode, said programmable conductance element having a resistance which is controllable between two states; and

a second conducive layer over said programmable conductance element.

27. The device of claim 26, wherein said programmable conductance element is comprised of a chalcogenide glass.

28. The device of claim 27, wherein said chacogenide glass is comprised of germanium-selenide.

29. The device of claim 27, wherein said chacogenide glass is comprised of Ge_xSe_{100-x}.

30. The device of claim 29, wherein x has a range of 18 to 43.

31. The device of claim 30, wherein x is 20.

32. The device of claim 26, wherein said chacogenide glass is doped with a metal.

33. The device of claim 26, wherein said chacogenide glass is doped with silver.

34. The device of claim 26, wherein said first and second conductive layers are comprised of one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

35. A processor based system, comprising:

a processor;

a memory device, said memory device including a plurality of memory cells,

wherein each of said memory cells comprises,

a substrate, the substrate having a source region and a drain region;

a first insulating layer over said substrate;

a first conductive layer over said first insulating layer;

a programmable conductance element over said first electrode, said programmable conductance element having a resistance which is controllable between two states; and

a second conductive layer over said programmable conductance element.

36. The device of claim 35, wherein said programmable conductance element is comprised of a chalcogenide glass.

37. The device of claim 36, wherein said chacogenide glass is comprised of germanium-selenide.

38. The device of claim 36, wherein said chacogenide glass has a chemical formula of Ge_xSe_{100-x}.

39. The device of claim 38, wherein x has a range of 18 to 43.

40. The device of claim 39, wherein x is 20.

41. The device of claim 36, wherein said chacogenide glass is doped with a metal.

42. The device of claim 36, wherein said chacogenide glass is doped with silver.

43. The device of claim 35, wherein said first and second conductive layers are comprised of one of tungsten, nickel, tantalium, aluminum, platinum, and silver.

44. The memory cell of claim 1, wherein said programmable conductance element is a multi-layer structure comprised of:

a first layer comprising $Ge_{40}Se_{60}$;

a second layer, formed over said first layer, said second layer comprising,

at least one of,

a sublayer of Ag, and

a sublayer of Ag_2Se;

a third layer comprised of $Ge_{40}Se_{60}$;

a fourth layer, formed over said second layer, comprising Ag; and

a fifth layer, formed over said fourth layer, comprising $Ge_{40}Se_{60}$.

45. The memory cell of claim 26, wherein said programmable conductance element is a multi-layer structure comprised of:

a first layer comprising $Ge_{40}Se_{60}$;

a second layer, formed over said first layer, said second layer comprising,

at least one of,

a sublayer of Ag, and

a sublayer of Ag_2Se;

a third layer comprised of $Ge_{40}Se_{60}$;

a fourth layer, formed over said second layer, comprising Ag; and

a fifth layer, formed over said fourth layer, comprising $Ge_{40}Se_{60}$.

46. The system of claim 35, wherein said programmable conductance element is a multi-layer structure comprised of:

a first layer comprising $Ge_{40}Se_{60}$;

a second layer, formed over said first layer, said second layer comprising,

at least one of,

a sublayer of Ag, and

a sublayer of Ag_2Se;

a third layer comprised of $Ge_{40}Se_{60}$;

a fourth layer, formed over said second layer, comprising Ag; and

a fifth layer, formed over said fourth layer, comprising $Ge_{40}Se_{60}$.